THAT WHICH IS CLAIMED IS:

1. Data storage device comprising several registers that can be addressed by address words, and connected to p output ports through connecting means that can be configured in response to address words of p registers selected to read the contents of these registers on the p ports respectively, characterized in that all register address words (MAD) contain a specific bit with a predetermined rank (A) identical for all address words and remaining bits (b0, b1, b2), the registers are connected in pairs on each output port, each pair of registers containing two registers with address words that only differ in the value of the said specific bit, and by the fact that for each pair of registers and for each output port, the connecting means comprise a pair of first switching means (OITA0.0, OITA8.0) that can be controlled in a complementary manner by the specific bit in the address word of one of the two registers, and a second switching means (OITB0.0) connected to the output port considered (PL0.0) and that can be controlled from the remaining bits of the address words of the two registers, the first two switching means being connected firstly between the corresponding two registers (R0.0, R8.0), and secondly between the corresponding second switching means (OTTBO.0).

2. Device according to claim 1, characterized by the fact that the registers comprise m memory points so as to store data with m bits, and by the fact that the first switching means associated with a register (R0.0) in a pair comprises m first elementary path gates

(OITA0.0) connected to the corresponding m memory points in the register, by the fact that the first switching means associated with the other register (R8.0) in the pair comprises m other first elementary path gates (OITA8.0) connected to the corresponding m memory points of this other register, a first elementary path gate (OITA8.0) connected to a memory point of the register being controlled in a complementary manner with respect to the other first elementary path gate (OITA8.0) connected to the corresponding memory point of the other register, and by the fact that the second switching means comprises m second elementary path gates (OITB0.0), connected between the said output port considered and m pairs formed from the first elementary path gates and the other first elementary path gates, respectively.

3. Device according to claim 2, characterized by the fact that it comprises a first elementary inverter (IVA0.0) connected between each memory point of a register and the p first elementary path gates associated with this register, and a second elementary inverter (OIVB0.0) connected between each second elementary path gate connected to an output port and the pair formed by the first elementary path gate and the other first elementary path gate associated with the other register in the pair of registers.

4. Device according to either of claims 2 and 3, characterized by the fact that each first elementary path gate, and each other first elementary path gate may be formed by pairs of complementary MOS transistors, the grids of the two opposite types of transistors belonging

respectively to the two pairs being connected together to enable complementary control of the first elementary path gate and of the other first elementary path gate.

5. Device according to either of the previous claims, characterized by the fact that the first switching means associated with the two registers in a pair are located close to each other.

6. Device according to either of the previous claims, characterized by the fact that it is made in the form of an integrated circuit.

7. Device according to either of the previous claims, characterized by the fact that it is controlled by a signal processing processor, in read.